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An Embedded Switched-Capacitor Z-Source Inverter with Continuous Input Currents

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***Abstract*—This paper presents a three-phase Embedded Switched-Capacitor Z-Source Inverter (ESC-ZSI) topology with continuous input currents. In the proposed ESC-ZSI, the continuous input currents can be achieved by embedding the dc sources into the symmetrical impedance network compared with a Modified Switched-Capacitor Z-source Inverter (MSC-ZSI). A detailed operation principle analysis of the proposed topology is introduced. Moreover, the boost ratio, the voltage gain and the voltage stresses of the power switch and capacitors are carried out to highlight the advantages of the proposed topology as compared with the conventional topologies. Finally, the simulation and experimental results are provided to validate the theoretical analysis.**

***Index Terms*—Impedance source inverter, Z-source inverter, embedded Z-source, continuous input current**

I. Introduction

Impedance (Z-) source inverters are being increasingly employed in power conversion applications since the invention of the Z-source inverter (ZSI) [1] and the quasi Z-source (q-ZSI) inverter [2] in the past 15 years. The traditional ZSI is shown in Fig. 1. The ZSI features that it has boost capability and inherent shoot-through protection abilities [3]–[5] compared with the traditional voltage source inverter. Moreover, the single conversion stage of the ZSIs can effectively decrease the system cost and improve the efficiency [6]–[8]. However, there are some limitations of the conventional ZSI, such as low boost factor, high voltage stresses across the capacitors and switches and discontinuous input current. To tackle these problems, many attempts have been made to improve the performance of the ZSIs.

The conventional ZSI has two capacitors and two inductors of identical values, as shown in Fig. 1. Notably, the high conversion ratios of the ZSIs are mainly dependent on the number of passive components and their arrangement. In [9], Fig. 2 shows a switched-inductor ZSI, where the switched inductor provides a voltage gain at the same shoot-through duty ratio compared with conventional ZSI. Moreover, to achieve a higher boost rating and low voltage stresses across the switching devices of the main circuit, series-connected SL or SC cells can be inserted into the topologies [10]–[12]. For instance, in [12], a modified topology with an SC impedance network (MSC-ZSI) was introduced, as shown in Fig. 3, which can achieve an even higher boost factor with a shorter shoot-through duration and a larger modulation index. However, a higher boost capability

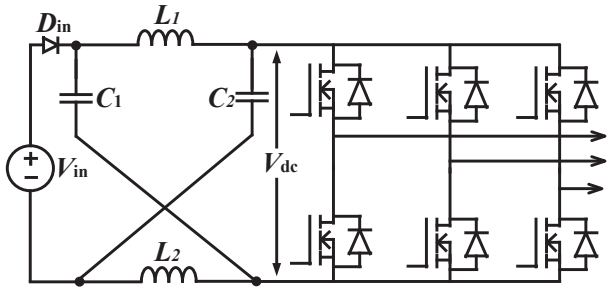

Fig. 1. Classic three-phase Z-source inverter, where V_{in} is the input DC voltage and V_{dc} is the DC-link voltage.

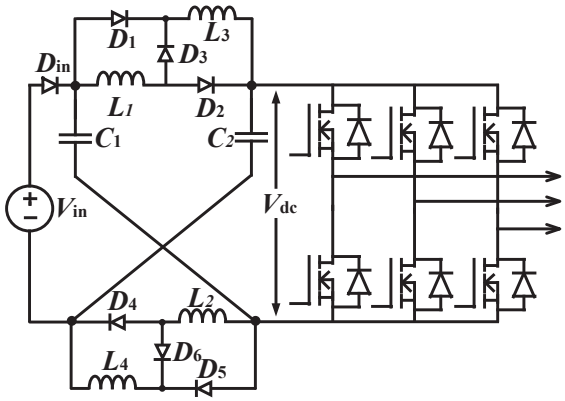

Fig. 2. Switched-inductor Z-source inverter [9].

is also achieved at the expense of cost and volume due to the extra inductors and capacitors.

Moreover, the dc current of the ZSI is usually discontinuous when the dc source is directly connected with the diode in the shoot-through state. To tackle this problem, the embedded ZSIs, where the dc sources are connected with inductors, were proposed in [13]–[15]. Fig. 4 shows a parallel-embedded Z-source inverter (E-ZSI), where the dc sources are embedded into the impedance network. The continuous input current can be achieved in this series connection between the dc sources and the inductors. Inspired by the above, a new Embedded Switched-Capacitor Z-source Inverter (ESC-ZSI) is then proposed in this paper. The proposed ESC-ZSI can achieve not only continuous input dc currents maintaining the same boost capability as the MSC-ZSI, but also lower stresses on the

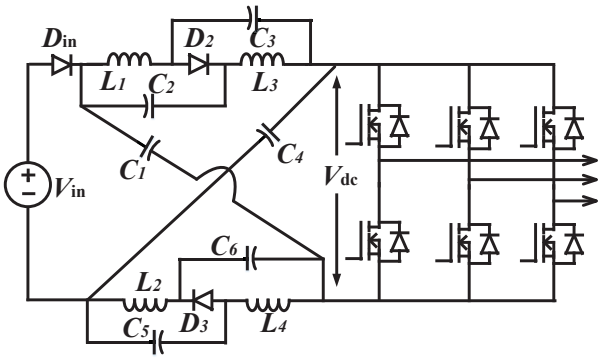

Fig. 3. MSC-ZSI topology [12].

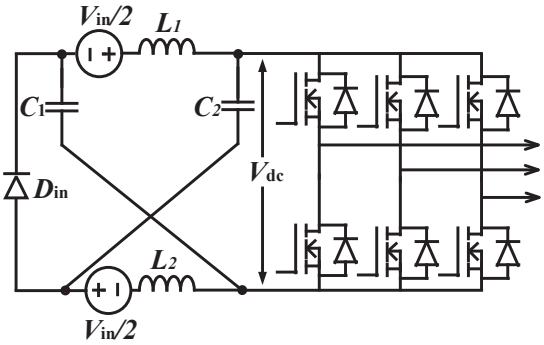

Fig. 4. Parallel-embedded Z-source inverter [13].

power devices. In Section II, the operation principle of the proposed topology is presented. Comparisons with the conventional switched impedance network and the proposed ESC-ZSI are performed, and benchmarking results are provided in Section III. Simulation and experimental results are given in Section IV, which verify the improved performance of the proposed topology in terms of continuous input dc current and lower stresses of the components. Finally, the paper is concluded in Section V.

II. Operation Principle of the Proposed ESC-ZSI Topology

The proposed ESC-ZSI is shown in Fig. 5, which has two symmetrical SC cells with embedded dc sources. The operation principle of the ESC-ZSI can be divided into two states–the shoot-through state and non-shoot-through state. The equivalent circuits of the proposed ESC-ZSI in the shoot-through state and non-shoot-through state are shown in Figs. 6 (a) and (b), respectively. It is assumed that all capacitors (or inductors) in the proposed topology are identical. Moreover, the embedded two dc sources are half of the input voltage before splitting, i.e., $0.5V_{\text{in}}$. The symmetrical topology leads to $i_{\text{L}_1} = i_{\text{L}_4}$, $i_{\text{L}_2} = i_{\text{L}_3}$, $V_{\text{C}_1} = V_{\text{C}_4}$, $V_{\text{C}_2} = V_{\text{C}_5}$, $V_{\text{C}_3} = V_{\text{C}_6}$, in which i_{L_1}, i_{L_2}, i_{L_3}, i_{L_4}, V_{C_1}, V_{C_2}, V_{C_3}, V_{C_4}, V_{C_5} and V_{C_6} are the corresponding currents through the inductor L_1, L_2 , L_3, L_4 and the voltages across the capacitor C_1, C_2, C_3, C_4 , C_5 and C_6.

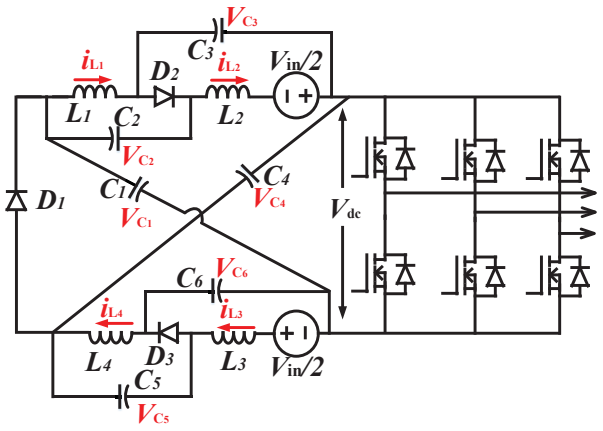

Fig. 5. Proposed three-phase switched-capacitor Z-source inverter.

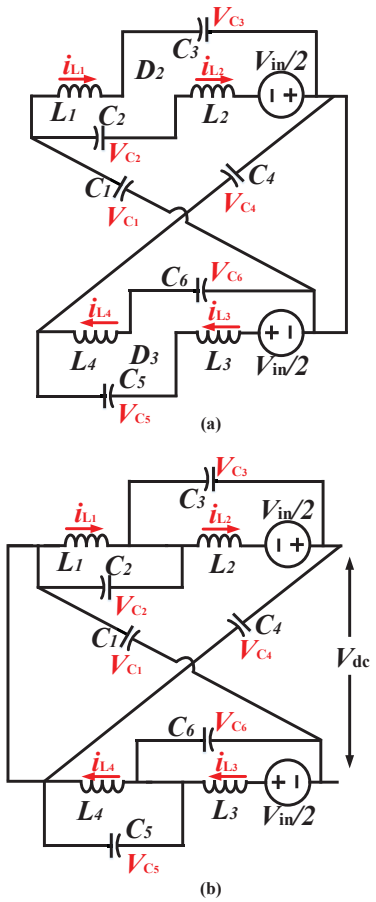

Fig. 6. Operation states for the proposed inverter (a) shoot-through state of the proposed Z-source inverter and (b) non-shoot-through state of the proposed Z-source inverter.

A. Shoot-Through State

As shown in Fig. 6 (a), three diodes D_1, D_2 and D_3 are all reverse-biased. In this case, the energy from the six capacitors is stored in the four inductors. The inductor L_1 is connected with C_1 and C_3 in series and the inductor L_2 is connected

with C_1, C_2 and one dc source in series. Then, according to the Kirchhoff's voltage law, it can be obtained that

$$V_{\text{L1-S}} = V_{\text{C}_1} + V_{\text{C}_3} \tag{1}$$

$$V_{\text{L2-S}} = V_{\text{C}_1} + V_{\text{C}_2} + V_{\text{in}} \tag{2}$$

in which $V_{\text{L1-S}}$ and $V_{\text{L2-S}}$ are the inductor voltages in the shoot-through state, and V_{in} is the dc-source voltage.

B. Non-Shoot-Through State

In the non-shoot-through state, as shown in Fig. 6 (b), three diodes are in ON state and the inductors then provide the stored energy to the ac load. During this state, the inductor voltages $V_{\text{L1-NON}}$, $V_{\text{L2-NON}}$ and the dc-link voltage V_{dc} can be represented by

$$V_{\text{L1-NON}} = -V_{\text{C}_2} \tag{3}$$

$$V_{\text{L2-NON}} = V_{\text{C}_2} - V_{\text{C}_4} + V_{\text{in}} \tag{4}$$

$$V_{\text{dc}} = V_{\text{C}_1} + V_{\text{C}_2} + V_{\text{C}_3} \tag{5}$$

It is known that the inductor average voltage in one cycle should be zero, and then applying the volt-second balance principle to all the inductors:

$$DV_{\text{L1-S}} + (1-D)V_{\text{L1-NON}} = 0 \tag{6}$$

$$DV_{\text{L2-S}} + (1-D)V_{\text{L2-NON}} = 0 \tag{7}$$

The capacitor voltages can be expressed in term of duty ratio, D and V_{in}.

$$V_{\text{C}_1} = \frac{1}{1-4D}V_{\text{in}} \tag{8}$$

$$V_{\text{C}_2} = \frac{2D}{1-4D}V_{\text{in}} \tag{9}$$

$$V_{\text{C}_3} = \frac{1-2D}{1-4D}V_{\text{in}} \tag{10}$$

The peak dc-link voltage V_{dc}^{p} and boost factor B can be derived from (8)-(10),

$$V_{\text{dc}}^{\text{p}} = \frac{2}{1-4D}V_{\text{in}} = BV_{\text{in}} \tag{11}$$

The peak output voltage V_{ac}^{p} of the inverter is expressed by

$$V_{\text{ac}}^{\text{p}} = \frac{MBV_{\text{dc}}}{2} \tag{12}$$

in which M is the modulation index. The buck-boost factor G can be expressed with respect to the modulation index as

$$G = MB = \frac{V_{\text{ac}}^{\text{p}}}{0.5V_{\text{dc}}} \tag{13}$$

TABLE I
BENCHMARKING OF SELECTED IMPEDANCE-SOURCE INVERTERS.

	ZSI [1]	E-ZSI [13]	MSC-ZSI [12]	ESC-ZSI
B	$\frac{1}{1-2D}$	$\frac{1}{1-2D}$	$\frac{1}{1-4D}$	$\frac{1}{1-4D}$
$\frac{V_{\text{s}}}{GV_{\text{dc}}}$	$2-\frac{1}{G}$	$2-\frac{1}{G}$	$\frac{4}{3}-\frac{1}{3G}$	$\frac{4}{3}-\frac{1}{3G}$
$\frac{V_{\text{C}_1}}{GV_{\text{dc}}}$, $\frac{V_{\text{C}_4}}{GV_{\text{dc}}}$	NA	NA	$\frac{4}{3}+\frac{2}{3G}$	$\frac{4}{3}-\frac{1}{3G}$
$\frac{V_{\text{C}_2}}{GV_{\text{dc}}}$, $\frac{V_{\text{C}_5}}{GV_{\text{dc}}}$	NA	NA	$\frac{2}{3}-\frac{2}{3G}$	$\frac{2}{3}-\frac{2}{3G}$
$\frac{V_{\text{C}_3}}{GV_{\text{dc}}}$, $\frac{V_{\text{C}_6}}{GV_{\text{dc}}}$	NA	NA	$\frac{2}{3}-\frac{2}{3G}$	$\frac{2}{3}+\frac{1}{3G}$

III. COMPARISON OF THE PROPOSED ESC-ZSI WITH OTHER TOPOLOGIES

In order to validate the performance of the proposed ESC-ZSI, a detailed benchmarking is performed, and the results are shown in Table I. Fig. 7 shows how the boost factor changes with the shoot-through duty ratio among benchmarked these topologies. It is further observed that in Fig. 7 the proposed ESC-ZSI and MSC-ZSI have a higher boost factor than the ZSI and the E-ZSI. In addition, the comparison of voltage gains among the selected topologies is shown in Fig. 8, where the voltage gain of the ESC-ZSI and MSC-ZSI is much higher than the E-ZSI and ZSI. Moreover, it can be seen in Fig. 9 that the power switch stress of the proposed ESC-ZSI is the same as the MSC-ZSI but much lower than the ZSI and E-ZSI for the same voltage gain. It is worth noting that the lower power rating of the switches can lead to lower cost. In addition, Fig. 10 shows that although the voltage stresses of the capacitors are not exactly the same in the MSC-ZSI and the ESC-ZSI, the sum of the stresses for all the capacitors of the ESC-ZSI is not affected in the embedded topology.

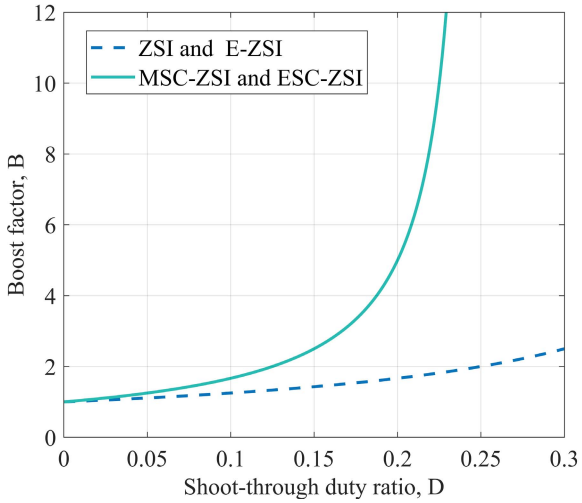

Fig. 7. Boost factor comparison of the three Z-source inverters (i.e., the ZSI, E-ZSI, and MSC-ZSI) with the proposed ESC-ZSI.

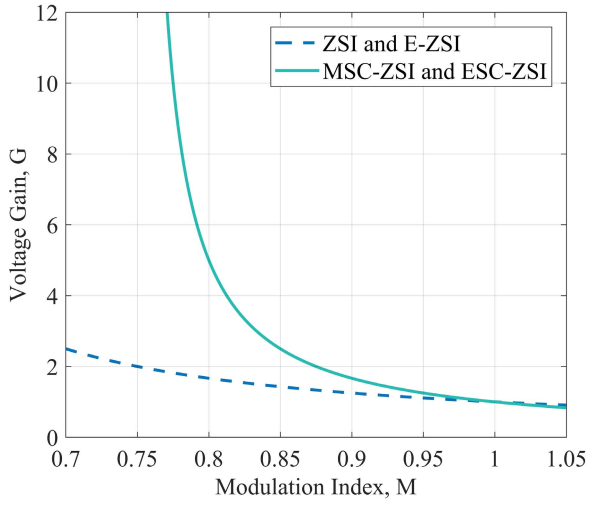

Fig. 8. Voltage gain comparison of the three Z-source inverters (i.e., the ZSI, E-ZSI, and MSC-ZSI) with the proposed ESC-ZSI.

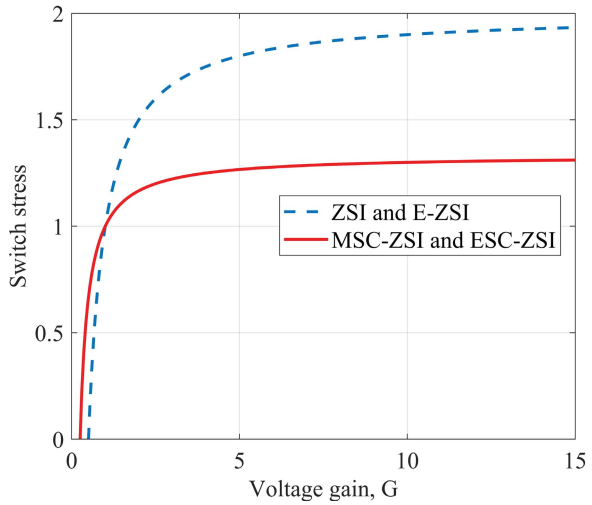

Fig. 9. Switch stresses comparison of the three Z-source inverters (i.e., the ZSI, E-ZSI, and EB-ZSI) with the proposed ESC-ZSI.

IV. Simulations and Experimental Tests

To further demonstrate the proposed ESC-ZSI, simulations and experimental tests are performed. Parameters of the inverter are shown in Table II.

A. Simulation Results

The proposed ESC-ZSI is simulated in the PLECS and MATLAB/Simulink environment with an open-loop control. The simulation results are shown in Fig. 11 under the condition $M = 0.8$ and $D = 0.175$. According to (9), the boost factor is calculated as $B = 3.33$, and thus the boosted dc-link peak voltage should be 100 V. Based on the operation principle during the shoot-through state, the inductor currents increase when the dc-link voltage is short-circuited, as shown in Fig. 11 (b). It can be seen from Fig. 5 that the two dc sources are directly connected the inductors L_2 and L_3, so the dc input currents are also inductor currents, which means that the DC currents are also continuous, and the peak dc-link voltage V_{dc} is almost boosted to 100 V, as expected. Moreover, as it can be seen in Fig. 11 (c), the capacitor voltages V_{C_1}, V_{C_2}, V_{C_3}, V_{C_4}, and V_{C_5} are, respectively, boosted to 50 V, 17.5 V, 32.5 V, 50 V, 17.5 V, and 32.5 V. All the simulation results are in agreement with the theoretical analysis.

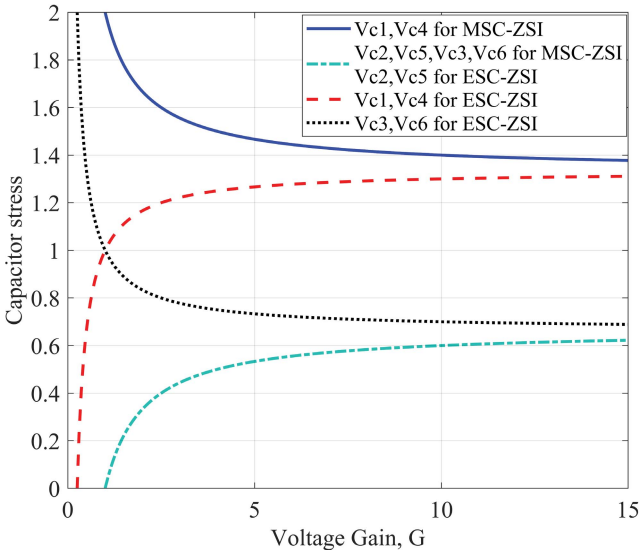

Fig. 10. Capacitor stresses comparison of the MSC-ZSI and the proposed ESC-ZSI.

TABLE II
Parameters of the Proposed ESC-ZSI in Simulations and Experiments.

Parameter	Symbol	Value
dc input voltage	V_{in}	30 V
ESC-ZSI inductance	L	640 μH
ESC-ZSI capacitor	C	100 μF
Load inductance	R_f	3 mH
Load resistance	L_f	30 Ω
Switching frequency	f_s	10 kHz

B. Experimental Results

An experimental setup is built up to verify the performance of the proposed ESC-ZSI and the experimental prototype is shown in Fig. 12. The experimental setup parameters are the same as simulation parameters. The switching signals are generated by a digital signal processor (DSP) TMS320F28335.

The experimental results are shown in Fig. 13. It is observed in Fig. Fig. 13 that the currents of the inductors L_2 and L_3, that is, the currents from the dc sources are continuous. Moreover, the results show that the dc-link voltage is boosted from 30 V to 96.8 V and V_{C_1}, V_{C_2}, and V_{C_3} are maintained at 47.8 V, 16.5 V and 31.2 V, respectively. It is known that the parasitic parameters of the inductors and capacitors, and the voltage drops of the diodes may affect the voltage gain. As

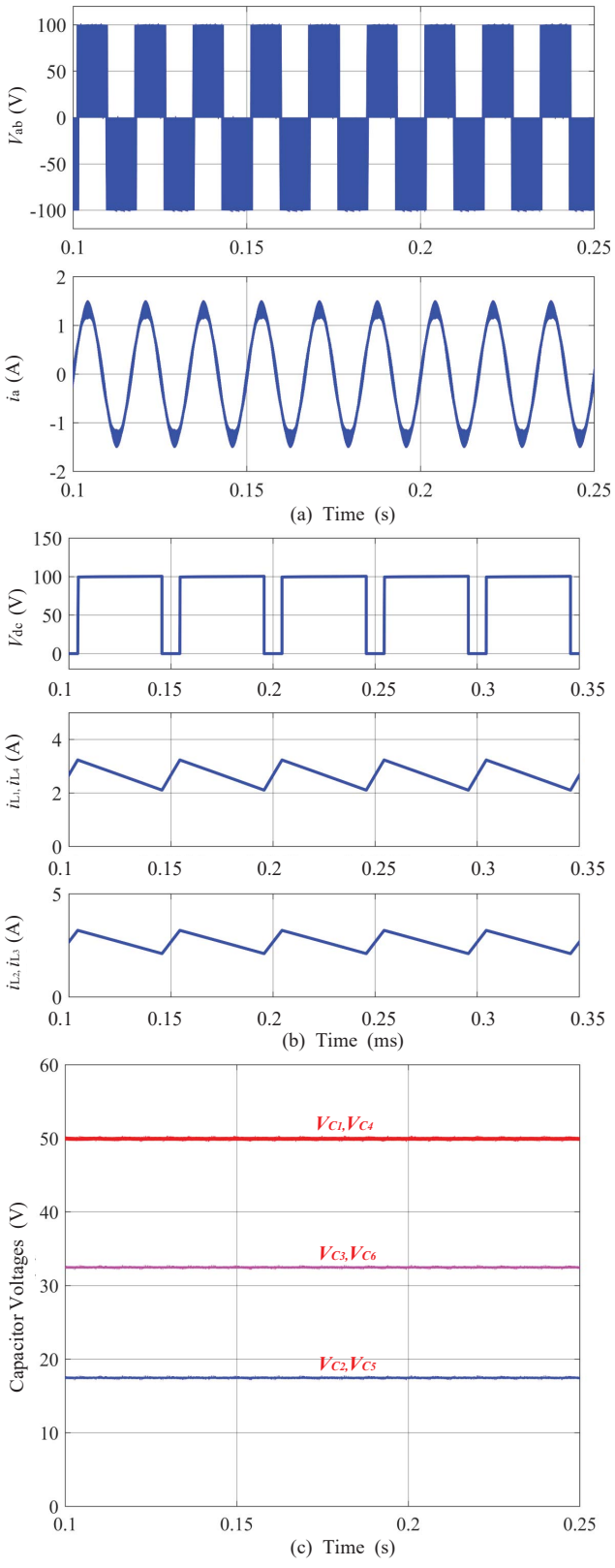

Fig. 11. Simulation results of the proposed ESC-ZSI, (a) the output leg voltage and load current in ESC-ZSI, (b) the dc-link voltage and inductor currents in ESC-ZSI, and (c) the voltages of the capacitors in the ESC-ZSI.

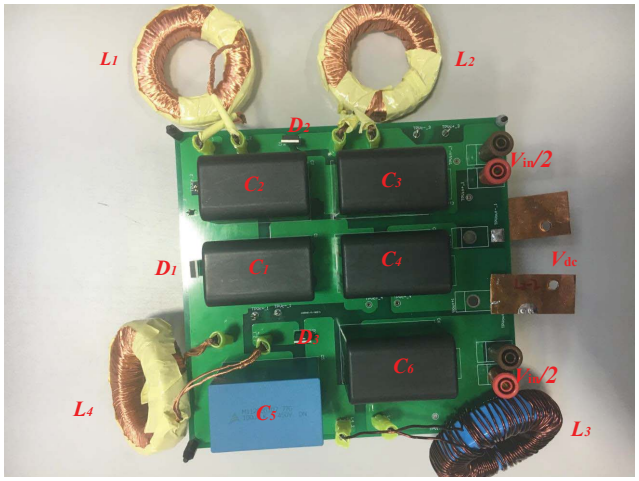

Fig. 12. Experimental prototype of the proposed ESC-ZSI topology.

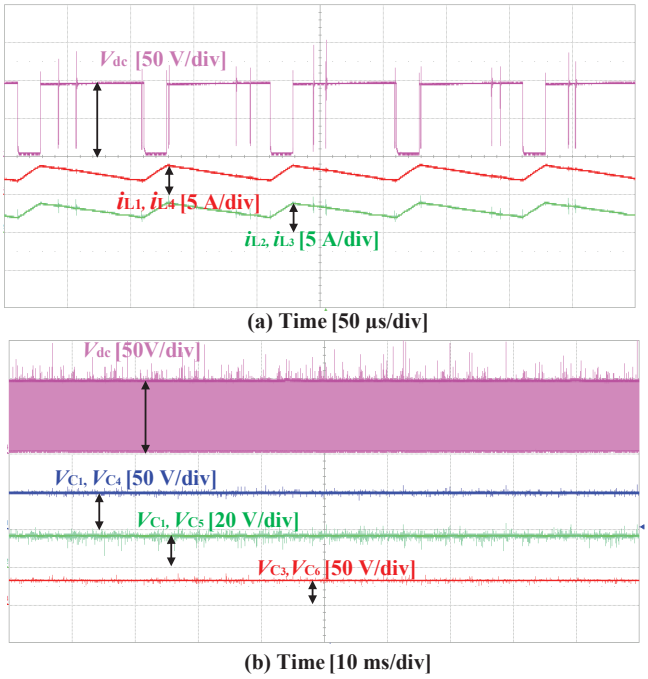

Fig. 13. Experimental results of the three-phase ESC-ZSI system: (a) the dc-link voltage V_{dc} and inductor currents i_{L_1}, i_{L_2}, i_{L_3}, i_{L_4} and (b) the dc-link voltage V_{dc} and capacitor voltages V_{C_1}, V_{C_2}, V_{C_3}, V_{C_4}, V_{C_5}, V_{C_6}.

a consequence, the voltages achieved in the experimental tests are slightly lower than those in the simulation cases.

V. Conclusion

In this paper, an Embedded Switched-Capacitor Z-Source Inverter (ESC-ZSI) was proposed. Compared with the traditional embedded ZSI and switched-capacitor ZSI, the current from the dc sources in the proposed topology can be continuous without affecting the boost ratio. Although two dc sources are embedded into the symmetrical topology, the stresses of the power switch are lower than those of the MSC-ZSI and the total capacitor stresses are the same as those in the MSC-ZSI.

Simulation and experimental tests have demonstrated that the proposed topology has a good boost capability and achieves continuous input currents.

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